Synthesis Technology E102 Quad Temporal Shifter
User Guide Version 1.0

Dec. 2014
www.synthtech.com/euro/e102

OVERVIEW

The Synthesis Technology E102 is a digital implementation of the classic Analog Shift Register (ASR). Features include:

- No droop, 14-bit accurate conversion
- Quantizer
- CV-controlled delay between stages (up to 511 clocks/stage)
- Digital noise generator with CV-controlled spectra
- Internal clock generator

The term Analog Shift Register (ASR) comes from the original Serge module name: an ASR is essentially a clocked delay for CVs. The E102 acts like four cascaded Sample & Hold modules, but its unique feature-set allows it to add time delay in-between each Sample & Hold stage. Since the sampled Control Voltages are digitized and stored in memory they can be delayed as long as required. The extent of the time to shift from one stage to the next depends on the clock speed, but there is no lower limit. When used with VCOs, the E102 is great at producing trills and musical canons out of a single CV source. Of course its use is not limited to driving VCOs only, clocking the module really fast will allow for delays of envelopes, Gates and LFOs.

The noise generator provides CVs from the outputs without requiring that the user supplies a CV at the input. If the INPUT is unpatched, the Digital Noise Generator is internally connected to the ASR. This turns the module into a unique four-output shift registered Sample & Hold. Changing the spectra of the Digital Noise will create new sequences/arpeggiations from the outputs.

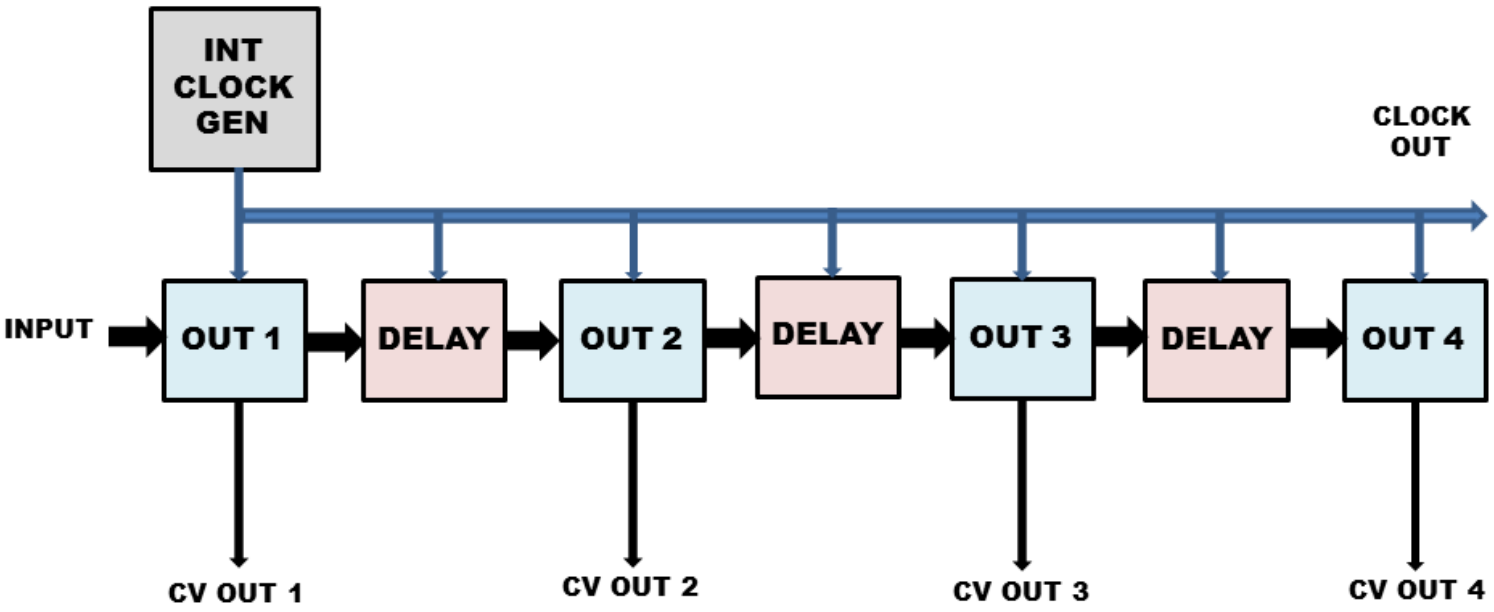


Figure 1: Simplified Block Diagram

The clock can be the internal RATE or an externally patched clock. There are optional DELAY stages in-between OUT 1 and OUT2, OUT 2 to OUT 3 and OUT 3 to OUT 4.

The delay stages shown in Figure 1 are the E102's variable sample clock delays, using the DELAY control and the 3 position range switch. However, the relationship between the INPUT CV, OUT 1 and the sample clock is unique and explained in depth in the SAMPLING CONSIDERATIONS section.

This type of arrangement is called a shift register. In the digital logic equivalent, the stages are flip-flops. The Moog 960 sequencer (and many modern hardware sequencers) use digital shift registers. Each clock will "turn on" the next stage of the sequencer. If you are familiar with hardware sequencers, then you already know how the E102 is internally connected! Instead of "stages" of a sequencer, the E102 has "memory locations" that are used to store the sampled voltage input.

SHIFT REGISTERS

Let us consider a simple example of how the ASR works. Say we send 1V on the input of the E102, using the internal clock, with no delay engaged between the Shift Register stages. After the first 1Volt sample the input is removed, exactly like momentarily pressing a key on a controller and letting go.

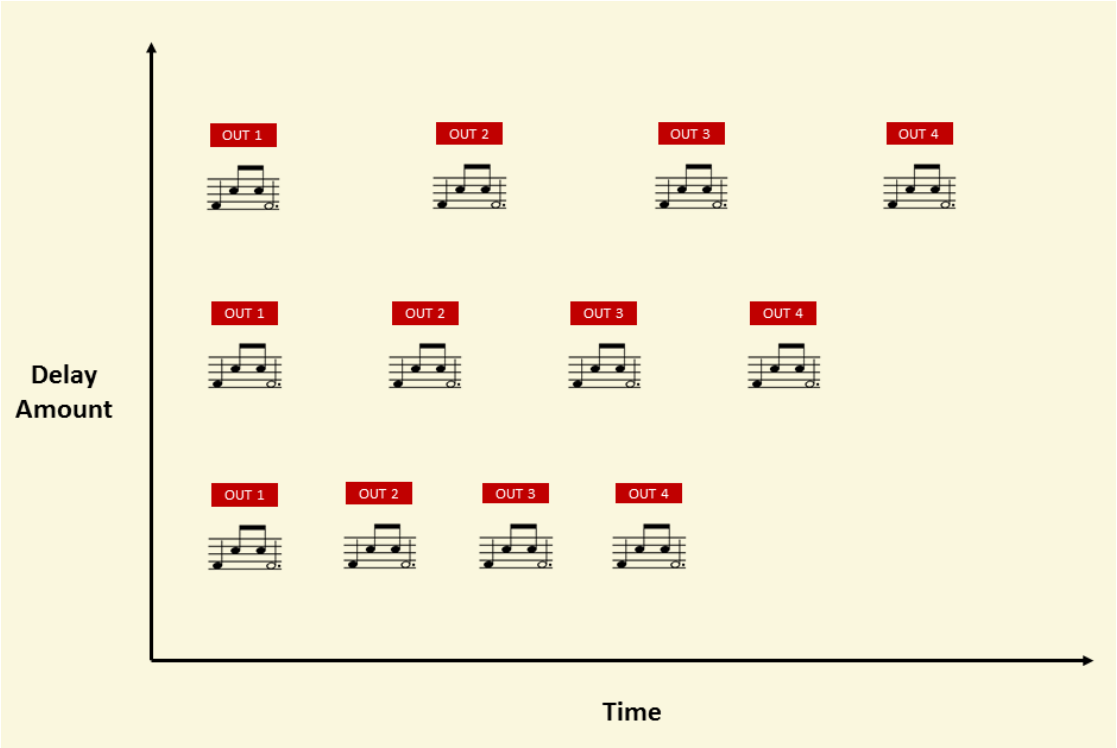
CLOCK	*OUT 1*	*OUT 2*	*OUT 3*	*OUT 4*
1	**1 Volt**	0 Volts	0 Volts	0 Volts
2	0 Volts	**1 Volt**	0 Volts	0 Volts
3	0 Volts	0 Volts	**1 Volt**	0 Volts
4	0 Volts	0 Volts	0 Volts	**1 Volt**

Notice how the 1Volt sample is "shifting over" stage-to-stage with each clock pulse. If each output of the module is assigned to a different VCO then the module captures the incoming CV voltage and passes it to the four outputs, essentially moving the note information between the four voices with each clock pulse received. Just as important, see how the 0 volts is also shifted into the memory after the first clock. The shift register will convert on every clock, no matter what the INPUT voltage is. The INPUT is sampled every clock.

The is only one 'direction' to shift, from OUT 1 to OUT 2 to OUT 3 to OUT 4. Most sequencers allow you to shift 'forwards' or 'backwards' or even 'random'. The E102 can be thought of as always shifting 'forwards'.

Now to make things a bit more complex let us say that a CV sequencer module is plugged in the E102 input and a small sequence of CVs is created, giving product to a series of notes. For the sake of convenience in our example both the E102 and the sequencer will be using the same clock source; this means that the RATE of the clock is the same for both modules.

We will symbolise the sequence of notes coming from the sequencer as: 



Notice how the sequence of notes is repeated in time sequentially on the four outputs. By increasing the amount of DELAY between the stages, it takes a larger amount of time for the sequence to be outputted from each stage. Remember that the E102 and the CV sequencer use the same clock source, so the RATE of the clock is constant. This allows for the time relationship between the notes of the sequence to remain identical regardless of the amount of applied DELAY.

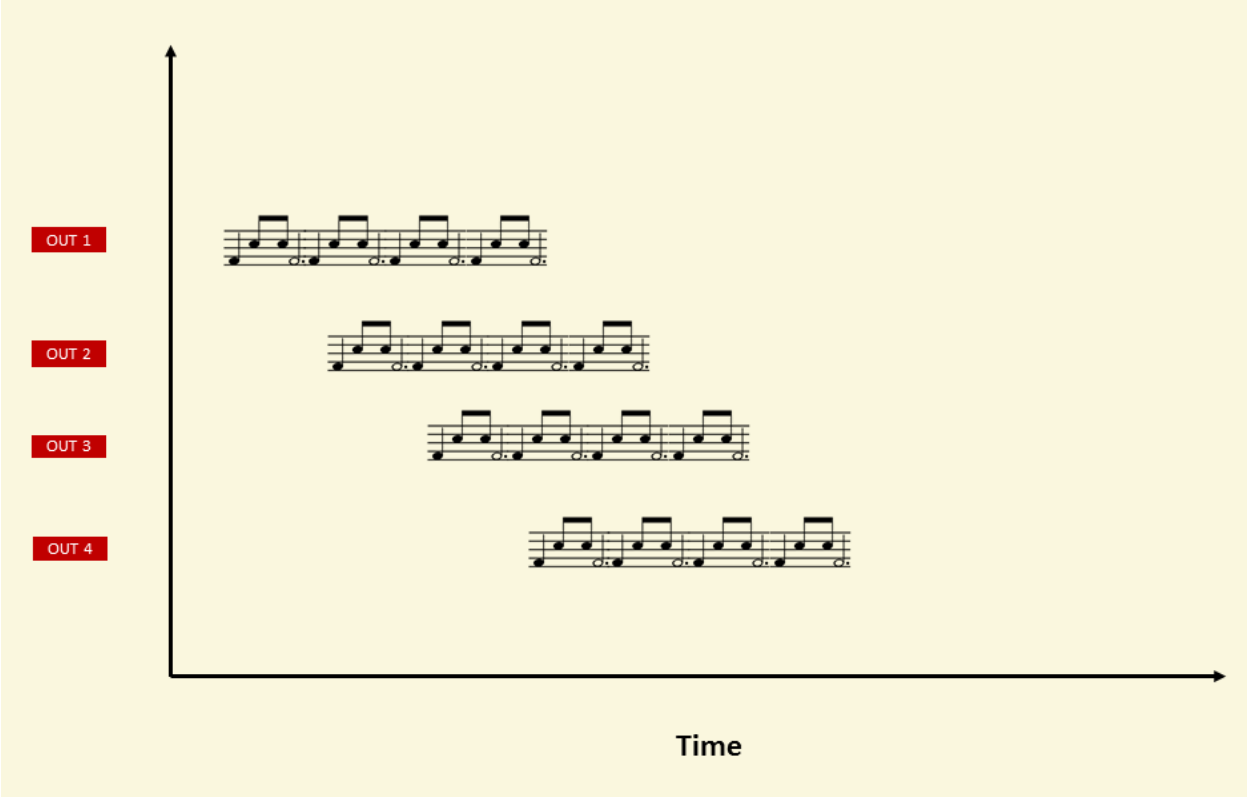
The DELAY concept is unique to the E102, and can be a bit confusing. It is important to understand that the DELAY is not a “clock divider”. If the DELAY = 4 clocks, what this means is a certain series of notes (like the 3 shown above) will appear successively at the four OUT jacks every 4 clocks. However, EVERY CLOCK SAMPLES THE INPUT AND LOADS IT VALUE INTO THE SHIFT REGISTER. There is no ‘silence’ or ‘pause’ in-between the patterns. The DELAY will extend the number of sample clocks in-between the output stages. This is called an ‘elastic buffer’: think of it like the old toy spring ‘Slinky’. You can stretch out the E102 shift register length from 4 to 1533 clocks long. The 4 OUTs are simply ‘taps’ into the buffer.

The ‘blank spaces’ in the above diagram will have notes as well, just not necessarily the 3 notes shown. This diagram is just used to show how note patterns travel “down the line” in the shift register memory and adding delay means more clocks are required until these 3 specific notes appear at each output jack.

When using larger sequences and in dependence with the amount of DELAY applied, the outputted CVs can overlap in time, the created melodies intertwining into

musical canons; all of this coming from a single CV sequence.

When using an external sequencer with the E102, it is useful to first set DELAY equal to the number of notes in the repeating sequence. If you have an 8 note sequencer, set DELAY = 8. This will seem more “musically obvious”, as the CV pattern will repeat out at the OUT jacks, in order, at the exact same time as the sequencer repeats. Decreasing DELAY will then cause the ‘overlap’ as shown below.



The diagrams of these notes imply different note lengths, but in reality the note ‘duration’ is the period of the clock. If the internal clock is used, then all the notes generated are of equal length. The circuitry in the E102 samples the INPUT CV and updates all 4 OUT jacks only when there is a rising edge of the clock. The clock can be a LFO, the Trigger out of a drum machine, or even an Envelope. Remember, the period/frequency of the clock sets the note “on time”, not the clock’s duty cycle.

CLOCKING THE E102

The E102 samples the INPUT jack and updates the shift register contents each rising edge of the clock. The width of the ‘hi’ portion of the clock needs to be at least 450ns. In most cases, the applied clock has a 50-50 duty cycle, but this is not required. The clock is generated by default by the E102 and is internally routed to a switched contact on the CLOCK IN jack. The internal clock is also sent to the CLOCK OUT jack as a 0 to 6.5V square wave. The CLOCK OUT can be used to synch sequencers, reset LFOs or trigger EGs.

Many signals can be used to externally clock the E102, because the circuitry has a threshold comparator. The comparator is set to treat any CLOCK IN voltage over 0.65V as a “clock is high” signal. Any applied voltage below 0.65V is read as “clock is low”. This allows just about any signal to be used to clock the E102. The voltage must be restricted from -10V to +10V on the CLOCK IN jack.

The internal clock generator is set for a range from 0.5Hz to 925Hz, roughly 1V/Oct (uncalibrated, but pretty close). There is no limit on the lower clock range. The E102 uses static RAM to store the digitized voltages. As long as power is applied, the voltages are saved and retained. You can stop the clock and start it again and the shift register will “freeze in position”, starting out where it left off when more clocks are applied.

The upper range of the clock is around 4,000Hz and is limited by the speed the processor can run the code and update the hardware. The low-pass noise filter will limit sampling AC signals to ~100Hz (see SAMPLING CONSIDERATIONS below).

High clock rates and longest delays are useful for delaying envelopes and LFOs. The E102 is a sampled system, using 14-bit converters. So, there will be some “stair-stepping” when trying this. But the output voltage steps are quite small (on the order of 500uV/step) so it is doubtful these tiny steps are audible for EGs or LFOs. Gate delaying is easy and straightforward using the E102. When used as a ‘straight CV delay’, use OUT 4 to get the most delay time and delay range.

SAMPLING CONSIDERATIONS

INPUT CV NOISE FILTER

The CV to be sampled is patched to the INPUT jack, or if unpatched the Digital Noise is used. In either case, the voltage is fed to a 14-bit accurate A/D converter and passed to a software low-pass filter. The cutoff frequency of this filter is ~250Hz at -6dB/octave. The filter is used to remove noise and to give time for the input CV to ‘settle’ to a stable value. It also mimics the behaviour of a traditional analog ASR made from cascaded S&H stages using analog switches and storage capacitors. The analog ASR has a small but finite “acquisition time” to charge the capacitors to a stable value, once the clock is received. Analysis of several commercial analog ASRs confirmed the E102’s software filter closely mimics the analog nature of these analog ASRs.

RELATIONSHIP OF INPUT CV, OUT1 AND CLOCK

It was stated earlier the E102’s DELAY stages are not present for INPUT to OUT1. However, it is important to understand what the voltage present at OUT1 is in relationship to the INPUT CV and the sample clock.

*The easiest way to think of the OUT1 voltage relationship is that it is the stored value of the INPUT CV **prior to** the last rising clock edge.*

Why is this?

The E102 uses the rising edge of the clock to sample, and the actual time to detect the edge, sample and update OUT1 is very fast, on the order of 200ns. But recall the noise filter is "in front" of the sample clock and it has a much longer rise/fall time of a few 100us.

This means that when using an externally clocked and CV generated system (like a sequencer), the sequencer's CV output will be updated faster with respect to its clock than the E102's noise filter + sample time. This means the E102 samples into OUT1 (and hence into the shift register) not the voltage immediately generated by the sequencer, but the voltage 1 clock prior.

This is where the 1 clock difference lies between the sequencer's CV output and the E102's OUT1 voltage.

Now, this may at first appear 'broken' or 'incorrectly implemented' but this is exactly how legacy analog ASRs work. The CMOS analog switch resistance and the S&H hold capacitor form a low-pass RC filter and since the S&H caps cannot change voltage instantly, they have to slew to the 'correct' voltage and this take place *after* the shift clock has occurred. The E102 copies this exactly.

Therefore, OUT1 will "lag" one clock period behind the sequencer's CV output with respect to the sequencer's clock. Using only the E102's outputs and not the sequencer's CV out, 'removes' the clock slew. Also remember that adjusting the notes on the sequencer means listening to OUT 1 's VCO and setting the note on the ***prior*** sequencer stage that is shown "active".

It is easier "musically" to just use the E102's CV OUTs only to drive the VCOs and not the sequencer's CV out. In this manner, OUT1 is the "original sequence" and OUT2-OUT4 are the "delayed versions of the sequence".

Here is another way to think about this skew. If you have an 8-stage sequencer clocking the E102 that is not running and Stage 1 is active, the CV for that stage is present on the sequencer's output. But that voltage happened after the prior sequencer clock. The sequencer's internal shift register either reset to stage 1 or advanced from stage 8 back to stage 1, but it happened 'in the past'. If this voltage is applied to the INPUT of the E102, it doesn't appear at OUT1 because no clock has been received by the E102. The sequencer is idle. Now if you run the sequencer, the next clock advances to stage 2 while simultaneously sampling the stage 1 voltage into the E102. The E102 will wait for the next sequencer clock, which shifts OUT1 to OUT2 and loads Stage 2 into OUT1. Now, you may be saying "But the voltage changed when the sequencer advanced!" and you are correct, but it was not instantaneously. The sequencer clock occurred, the logic had to advance and the

voltage had to appear. Then, our 'front end' filter has a time constant and by the time the next stage voltage is stable, the E102 has loaded in the older, prior stage's voltage which relatively speaking, has been stable for a long time.

PROPER CLOCK RATE

The internal clock is used when nothing is patched into CLOCK IN. The RATE of the sample/shift clock needs to be at least twice as fast as the INPUT CV is changing, preferably around 10 times as fast. For example, if you are sampling an arpeggiations out of a MIDI-CV converter that is cycling the notes at 4Hz, the RATE of the E102's internal clock should be 40Hz or greater.

The DELAY range and panel pots can be used with the 4 OUTs to set the desired overall "arpeggiator delay time". This is where the E102's longer DELAY setting is very useful. Even fast-changing INPUT CVs, like LFOs and envelopes, can be delayed 100s of milliseconds with fast RATE settings. Remember, OUT 4 has 3 delay stages from INPUT to OUT 4, and at the longest setting are 511 each. Sampling at the fastest internal RATE of 925Hz is still over a 1.5 second overall delay from INPUT to OUT4. The fast sample clock/very long delay can be VERY useful in patching, especially when slowing modulating the DELAY CV.

The upper limit for driving into CLOCK IN is higher than the internal clock of 925Hz. External clock can be as high as 4KHz.

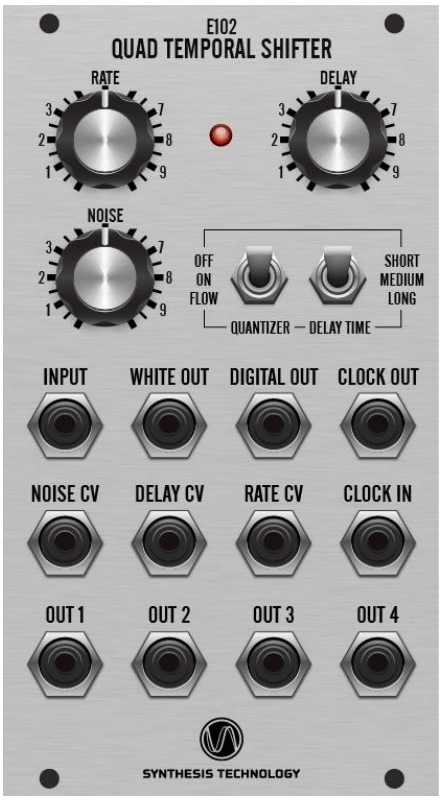
PROPER MODULATION ATTENUATION REQUIREMENTS

The parameters that respond to external CV (RATE, Digital Noise, DELAY) have an input range of -5V to +5V. However, it is important to understand that any applied CV is added to the panel control setting. Each corresponding panel control can be envisioned as going from -5V when fully counter-clockwise to +5V when fully clockwise.

This is why external attenuators, like the Intellijel TriATT are necessary when applying external modulation CVs. Most modulation sources, like an LFO, have -5V to +5V outputs. If this is patched into the E102 (say the RATE CV), this is equivalent to turning the RATE panel control "end to end", minimum rate to maximum rate. Unless the RATE pot is exactly in the center of rotation, the external CV will overload the circuitry.

For example, if the RATE pot is set at the "9:00 position", internally the circuitry is applying -3V to the controller. If you apply an attenuated -1V to +1V LFO into RATE CV, this is added to the -3V to result in a -4V to -2V RATE modulation. This is within the total -5V to +5V range. But if you 'crank up' the modulation to -3V to +3V, then there is a problem! The internal CV becomes -6V to 0V and -6V exceeds the limit. The circuity applied a "clamp" around -5V. What needs to happen is to move the RATE panel control to say 12:00 position. This is 0V for the panel RATE, the total rage shifts up to -3V to +3V and everything is OK. Think of the panel controls as the initial value.

CONTROLS



NOISE pot / NOISE CV input / DIGITAL OUT output / WHITE OUT output

Each noise algorithm gives a different flavour of digital noise at the DIGITAL OUT output. The NOISE pot and NOISE CV input both control the morphing from one flavour of noise to another. There are four types of digital noise available, from pings to pure pink noise. Specifically:

- **Metal Noise**
  This is "Crackle noise" run through a Karplus-Strong resonance algorithm

- **Crackle Noise**
  Impulses created when white noise exceeds a variable threshold

- **Clocked Digital Noise**
  White noise S&H at a variable rate

- **Pink noise**

Clocked Digital in the 50% - 75% range is has the widest spread of possible voltages to use as input for the delay line when random CV is desired.

INPUT

The CV to be sampled is applied here. There is an internal connection of the Digital Noise Generator when nothing is patched. The voltage range is -6V to +6V. This should be more than the “full range” of most modules, but please check what you are patching in before using. Some MIDI-CV converters can exceed +6V at the upper end of their range. A VCF in high resonance can also exceed +6V.

OUT 1 – 4 outputs

These are the CV outputs of the Analog Shift Register section of the module. OUT 1 provides the CV from the first stage and is the only one that has no DELAY applied to it, OUT 2 comes from the second stage, etc. The output stages use ‘cable driver’ circuitry to drive long patch cords and multiple loads with a CV voltage drop.

There trimmer on the E102 pc board is the scaling from INPUT to OUT CV. This should be 1:1 (a 4.000V input should be set for a 4.000V output). This is calibrated at the factory using a 6 ½ digit DVM.

QUANTIZER switch

The QUANTIZER switch has three positions:

- **OFF**
  When the switch is at the off position the OUT CVs are not quantized.

- **ON**
  When quantizer is engaged the CV of all four outputs is quantized to a 12-tone equal tempered scale; this is generally known as a chromatic scale. The scaling adheres to the 1V/Octave standard.

- **FLOW**
  At the flow position the input voltage is directly quantized and duplicated on the four outputs. So in essence this position acts as a bypass by disabling the ASR effects. Its intended purpose is for tuning individual VCOs or other modules as a set. You can also use the E102 as a ‘stand-alone’ quantizer while in FLOW mode. Any clocking is IGNORED in FLOW mode.

RATE pot / RATE CV input / LED / CLOCK IN input / CLOCK OUT output

In an ASR a clock is needed to shift the CV down the stages; for this purpose the E102 has an internal clock that is voltage controlled. The RATE pot and RATE CV input both control the rate with which the voltages are shifted in the ASR buffer, while an LED indicates the current rate. The same clock is used to sample the incoming CV

signal, so the RATE also controls the sample rate.

The CLOCK OUT output can be used to sync sequencers and other gear (Envelope Generators etc.) to the internal clock. Additionally the module can receive an external clock or LFO signal at the CLOCK IN input. Plugging a patch cord in that input disconnects the internal clock.

In ASRs one clock pulse equals one instance of the input CV being sampled and one shift of the stage, as both functions use the same clock.

DELAY pot / DELAY CV input / DELAY TIME switch

Adding DELAY spreads out the four stage outputs by adding memory buffer stages in-between the OUT stages. The shifter register is always filled and updates each clock pulse. The DELAY simply increases the number of clock pulses to 'travel down the chain'.

Remember that one clock pulse still equals one instance of the input CV being sampled, so the sample rate can by varied by changing the RATE parameter. In a typical delay unit the delay is in 'time' because the sample rate is constant, whereas on the E102 the sample rate is variable, meaning that the delay is actually in samples or clock pulses.

On the E102 the amount of DELAY is controlled by the DELAY pot or by an incoming CV at the DELAY CV input. The DELAY TIME switch defines the range of the DELAY in number of clocks between output stages:

- **SHORT =** 1-8 clocks
- **MEDIUM =** 1-32 clocks
- **LONG =** 1-511 clocks

It is worth pointing out that using the longest setting for the DELAY TIME switch while at the highest DELAY value will produce 511 clock pulses between each stage. This equals more than 1500 clock pulses between OUT 1 and OUT 4.

SIGNAL LEVELS

- INPUT CV to be sampled: -6V to +6V, 100Hz for full bandwidth
- CLOCK IN level: -10V to +10V
- CLOCK IN threshold for 'high': +0.65V +-5%
- CLOCK OUT voltage: 0V to +6.5V
- MODULATION CV range: -5V to +5V, but added to associated panel pot
- OUT1-4 accuracy: +-0.001V calibrated
- OUT1-4 voltage drift w/temperature: < 15ppm